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09/773,164	01/31/2001	Carsten Noeske	Micronas.5873	6108

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Samuels, Gauthier & Stevens LLP
Suite 3300
225 Franklin Street
Boston, MA 02110

EXAMINER	
DO, CHAT C	
ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/773,164	Applicant(s) NOESKE, CARSTEN
	Examiner Chat C. Do	Art Unit 2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: throughout the application, the term "multiplicant" is missed spelling. The term "multiplicant" should be "multiplicand".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 12-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 12, the limitation "the value ordered places" in line 4, "the canonical form" in line 8, "the output side" in line 9, and "the functions" in line 11 lack antecedence basis. For examination purposes, the examiner considers these limitation as "a value ordered places" in line 4, "a canonical form" in line 8, "a output side" in line 9, and "a functions" in line 11. In addition, it is unclear by what the limitation "a four-place adder" in line 10 means. For examination purposes, the examiner considers this limitation as just any adder.

Re claim 13, the limitation "the maximum number of places" in line 3 lacks an antecedence basis. The examiner considers this limitation as "a maximum number of places" in line 3.

Thus, claims 14-18 are also rejected for being dependent on the based claims 12-13.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Deutsch et al. (U.S. 4,031,377).

Re claim 1, Deutsch et al. disclose in Figure 1 a computing device on a monolithic integrated circuit for multiplying together a digitized multiplier signal value (C or output of 82) and a digitized multiplicand signal value (S or output of 81), computing device comprising: an input interface (81) that receives multiplicand and provides a received multiplicand indicative thereof (80); a first place shifting device (13) that includes a first logical assignment circuit to shift data bits of received multiplicand in response to a first shift command signal (17-21), and provides a first shifted signal indicative thereof (26); a second place shifting device (12) that includes a second logical assignment circuit to shift data bits of received multiplicand in response to a second shift

command signal (16), and provides a second shifted signal indicative thereof (25); means for summing (27) first and second shifted signals (A and B) to provide a summed signal value that is indicative of the product of multiplier and multiplicand (28'); and a control device (14) that receives a signal indicative of multiplier (15), and generates first (16) and second shift command signals (18-21) indicative of multiplier value.

Re claim 2, Deutsch et al. further disclose in Figure 1 a memory device for storing summed signal, and for providing past values of summed signal value (83).

Re claim 3, Deutsch et al. further disclose in Figure 1 means for summing receives and sums a signal value from memory device indicative of a past value of summed signal value with first and second shifted signals to provide summed signal value (83 acts as an accumulator to sum all the terms).

Re claim 4, Deutsch et al. further disclose in Figure 1 first place shifting device (13) comprises a first sign inverter (table III in col. 6) that receives and selectively inverts the sign of received multiplicand (S) to provide a second sign inverted received multiplicand signal that is input to first logical assignment circuit (13) for bit shifting (col. 5 lines 10-15 and table III in col. 6).

Re claim 6, Deutsch et al. further disclose in Figure 1 control unit (14) generates a first sign inversion command signal (17-19) in response to multiplier value, wherein first sign inversion signal is input to first sign inverter to selectively enable the sign inversion (table III in col. 6).

Re claim 7, it is a means claim of claim 1. Thus, claim 7 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 8, it is a means claim of claim 2. Thus, claim 8 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 9, it is a means claim of claim 3. Thus, claim 9 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 10, it is a means claim of claim 4. Thus, claim 10 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 12, it has all the limitations as cited in claim 1. In addition, Deutsch et al. further disclose in Figure 1 the functions such as place shifting, negation, and addition run as completed function (12, 13, 27, and 29) executions time-staggered in a pipeline process extending over at least two clock cycles.

Re claim 13, Deutsch et al. further disclose in Figure 1 the number of place shifting devices that can be controlled independently (14) of one another depends on the choice of the second number (table II and col. 6 lines 1-8), mainly on the maximum number of places of the second number, which is determined by this choice, the places with the value zero being excluded from the considered set of places (col. 6 lines 17).

Re claim 14, Deutsch et al. further disclose in Figure 1 the shift instruction for the particular place shifting device, a shift position is also defined for which the outputs for the following adder are blocked or are set to zero (col. 6 lines 4-7).

Re claim 15, Deutsch et al. further disclose in Figure 1 the output places of the adder (27) are coupled to the inputs of a summation memory (83).

Re claim 16, Deutsch et al. further disclose in Figure 1 a summation instruction activates a data path that correctly feeds back the place outputs of the summation memory to the adding inputs of the adder (83).

Re claim 17, Deutsch et al. further disclose in Figure 1 the first number (S) and the second number (C) are binary coded dual numbers (table III), and that the first and second number are multiplied by successive shift processes of a single place shifting device (12/13), the particular shift positions being determined by successive shift instructions, in dependence on the values of the associated binary places of the second number (C by 14).

Re claim 18, Deutsch et al. further disclose in Figure 1 if two or more place shifting devices are present (12 and 13), the successive shift processes take place by groups (shifting to output 25 and 26), in that a binary position of the second number (C by 14) is associated with each place shifting device (12 or 13), the associated binary positions of the second number being determined by successive shift instructions.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being obvious over Deutsch et al. (U.S. 4,031,377), as applied to claim 4 above, in view of Main (U.S. 5,402,369).

Re claim 5, Deutsch et al. do not disclose in Figure 1 a second place shifting device comprises a second sign inverter that receives and inverts the sign of received multiplicand to provide a sign inverted received multiplicand signal that is input to second logical assignment circuit for bit shifting. However, Main discloses in Figure 1 that the multiplier can be factored as multiple plus or minus terms in col. 5 lines 10-15. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an inverter in the first place shifting device as seen in Main's reference into Deutsch et al.'s reference because it would enable to compute the product faster and more efficient (without the first inverter, the system has to bypass the first place shifting device and subtract in the next clock using the second place shifting device).

Re claim 11, it is a means claim of claim 5. Thus, claim 11 is also rejected under the same rationale in the rejection of rejected claim 5.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,590,931 to Wittig discloses a reconfigurable FIR filter using CSD coefficient representation.

b. U.S. Patent No. 4,679,164 to Rearick discloses a digital high speed programmable convolver.

c. U.S. Patent No. 5,235,536 to Matsubishi et al. disclose an absolute difference processor element processing unit, and processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

July 11, 2003

CHUONG DINH NGO
PRIMARY EXAMINER